DETAILED ACTION

Claim Objections

Claims 6-7 recite the limitation "chip components" in line 1. There is insufficient antecedent basis for this limitation in the claims.

Claims 19-20 recite the limitation "the chip components" in line 1. There is insufficient antecedent basis for this limitation in the claims.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 5, 8, 11, 13, 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masashi et al. (JP. 2002-208668) in view of Ohmori et al. (U.S. Pat. 6166431).

- Regarding claims 1, 11 and 13, Masashi et al. disclose a semiconductor device comprising:

a semiconductor chip 2;

a wiring board 4 over which said semiconductor chip 2 connected by solder 5 is mounted;

a plurality of bonding wires 8 for connecting surface electrodes of said semiconductor chip to terminals of said wiring board corresponding thereto; and

a sealing section in which said semiconductor chip and said plurality of bonding wires are covered and sealed with resin, said sealing section being formed of an insulating elastic resin (cover fig., abstract), wherein said elastic resin has an elastic modulus of 200 MPa or less at a temperature of 150 degree C or higher (cover fig., paragraph 0027).

Masashi et al. do not disclose a height of said bonding wire from a main surface of said semiconductor chip (a bonding start point) to a top of said bonding wire is 0.2 mm or less.

However, Ohmori et al. disclose a semiconductor device comprising a height of a bonding wire 13 from a main surface of the semiconductor chip to a top of the bonding wire is 0.2 mm or less (cover fig., column 6, lines 24-26). Therefore, it would have been obvious to one having ordinary in the art at the time the invention was made to modify the device structure of Masashi et al. by having a height of said bonding wire from a main surface of said semiconductor chip to a top of said bonding wire is 0.2 mm or less as taught by Ohmori et al., such the 0.2 mm height of the wiring portion would provide a thin semiconductor device package (cover fig.).

- Regarding claim 2, Ohmori et al. disclose a height of said bonding wire 13 from the main surface of said semiconductor chip 11 to the top of said bonding wire is from 0.1 mm or more to 0.2 mm (cover fig., column 6, lines 24-26).
- Regarding claim 5, Masashi et al. disclose that the elastic resin is silicone resin (abstract).

- Regarding claim 8, Masashi et al. disclose that the elastic resin has an elastic modulus of 200 MPa or less (the elastic modulus of 5 to 10 MPa is in the range of 200 MPa or less) at a temperature of 150 degree C or higher (cover fig., paragraph 0027).
- Regarding claim 17, Masashi et al. disclose that the bonding wires 8 are made of gold (cover fig., paragraph 0066).
- Regarding claim 20, Masashi et al. disclose that chip components 3 are connected onto the wiring board by solder 5 (cover fig.).

3. Claims 3-4, 9-10, 12, 14 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masashi et al. (JP. 2002-208668) in view of Ohmori et al. (U.S. Pat. 6166431) and further in view of Hiroshi (J.P. 2000021920).

- Regarding claims 3-4, 10, 12 and 14, Masashi et al. in view of Ohmori et al. substantially disclose all the limitations as claimed above except for a wire horizontal distance from a bonding start point to an end point of the bonding wire is 1.5 mm or less.

However, Hiroshi discloses a semiconductor device comprising: a wire horizontal distance from a bonding start point to an end point of a bonding wire 7 is about 0.7 mm (fig. 4, paragraph 0031). Therefore, it would have been obvious to one having ordinary in the art at the time the invention was made to have a wire horizontal distance from a bonding start point to an end point of the bonding wire is about 0.7 mm as taught by Hiroshi into the device of Masashi et al. in order to improve the reliability of the chip to the wiring board (fig. 4).

- Regarding claim 9, Hiroshi discloses a recess 2 is formed in said wiring board 1 and said semiconductor chip 6 is disposed in said recess (cover fig.).
- Regarding claim 18, Masashi et al. disclose that the bonding wires 8 are made of gold (cover fig., paragraph 0066).
- Regarding claim 19, Masashi et al. disclose that chip components 3 are connected onto the wiring board by solder 5 (cover fig.).

4. Claims 6-7 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masashi et al. (JP. 2002-208668) in view of Ohmori et al. (U.S. Pat. 6166431) and further in view of Ono et al. (U.S. Pub. 2002-0110697).

Masashi et al. in view of Ohmori et al. substantially disclose all the limitations as claimed above and Masashi et al. further disclose chip components 3 having connection terminals formed on both ends thereof are connected to the wiring board 1 by solder 5 (cover fig., abstract) and the semiconductor chip 2 is connected to the mounting board by solder 5 (cover fig., abstract). Masashi et al. and Ohmori et al. do not disclose the solder is mainly comprised of tin (Sn) and antimony (Sb) or the solder is mainly comprised of tin (Sn), silver (Ag) and copper (Cu), and the solder does not contain lead (Pb).

However, Ono et al. disclose a semiconductor package comprising: a solder is mainly comprised of tin (Sn) and antimony (Sb) or the solder includes Sn-Ag-Cu, and the solder does not contain lead (Pb) (paragraph 0017). Therefore, it would have been obvious to one having ordinary in the art at the time the invention was made to form the solder is mainly comprised of tin (Sn) and antimony (Sb), and the solder does not

contain lead (Pb) as taught by Ono et al. into the device structure of Masashi et al. in order to eliminate the pollution against the natural environment and the human bodies (paragraph 0017).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 5:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hoai v Pham/
Primary Examiner, Art Unit 2814

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